Amendments to the Claims:

1-18 (Canceled)

19. (Currently amended) A unified system for transmitting and receiving data by a serial link across wired media, and comprising a transmitter and a receiver, the transmitter comprising:

a) phase locked loop control circuit having a digital coarse loop and an analog fine loop, the coarse loop including a reference generator, a voltage comparator, a PLL control logic, a digital ~~To~~ to analog counter and a low pass filter;

b) a two-stage voltage regulated ring oscillator controlled by the phase locked loop,

and capable of running at full bit frequency;

c) a frequency reference operating at one-fourth of full data rate;

d) a reference clock and a phase locked loop clock;

the fine loop control formed by a 4x frequency divider, a phase-frequency detector, a charge pump and a loop file; and

the receiver comprising a phase locked loop including a voltage controlled oscillator, a phase rotator independent of the phase locked loop and adapted to receive the output phases of the oscillator, a phase rotator control state machine for controlling the phase setting of a phase rotator and employing an over sampled half-rate system using a digitized early-late control .

20. (Currently amended) ~~In the~~ The unified system according to claim 19, wherein the transmitter and the receiver each includes a pseudo random bit stream generator and checker for self testing.

21. (Original) The system according to claim 20 wherein the transmitter architecture is supported by three analog blocks comprising the full data rate PLL, a phase buffer to repower the PLL signal for the driver and an off chip driver with a pre-emphasis equalization.

22- 23 (Canceled)